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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,149	08/31/2000	Garo J. Derderian	MI22-1330	4634

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WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
LE, THAO P	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

M'O

Office Action Summary	Application No.	Applicant(s)	
	09/653,149	DERDERIAN ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-25 and 34-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-25 and 34-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7 pages*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8, 10-25, 34-75 are pending.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 10/08/04, 03/11/05, 12/16/05, 12/21/05, 02/21/06 were filed after the mailing date of the application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Election/Restrictions

3. Applicant's traversal is fully considered. The previous election/restriction requirement has been withdrawn. Claims 1-8, 10-25, 34-75 are presented for further examination.

4. Examiner withdraws the 112 rejection made on 07/02/04.

5. Applicant's remarks made on 10/04/04 is fully considered, however, examiner disagreed with applicant's traversal that the "metal film disclosed in reference does not necessarily constitute forming a barrier layer to oxygen diffusion". The metal film in cited reference is formed by the same material and technique as the metal film of the present invention. Therefore, it is inherent that these two films carry out the same functions.

Claim Rejections

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8, 10-25, 34-75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzumi et al., U.S. Patent No. 6,222,722, and in view of Kim et al., U.S. Patent No. 6,207,487.

Regarding to claims 1, 34, Fukuzumi et al. discloses a method of forming a capacitor (See Fig. 33 and Cols. 1-20) comprising:

. forming a first capacitor electrode 51 over a substrate 1;

. forming a conductive barrier layer 52 over the first electrode (to prevent oxygen diffusion);

. forming a capacitor dielectric 53 over the barrier layer;

. forming a second capacitor electrode 54 over the dielectric layer.

Fukuzumi et al. fails to disclose the step of forming a conductive barrier layer using atomic layer deposition (ALD) technique. However, Kim et al. discloses the

method of forming capacitor including the step of forming conductive barrier layer over the first capacitor electrode using ALD method (abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Fukuzumi et al. in view of Kim et al. by using ALD to deposit conductive barrier layer over the first capacitor electrode because when ALD method is performed where a high-purity film is formed by a plurality of atomic layers so that various reactants necessary for deposition of the film are sequentially supplied to the substrate by a gas pulsing method, a film having perfect step coverage is achieved, the thickness of the film can be easily adjusted (lines 5-30, Col. 4), the leakage current at lower electrode is suppressed, electric potential of device acts strongly while capable of obtaining cell capacitance enough for device operation and lower a soft error rate (lines 35-40, Col. 2). The conductive barrier layer formed over the first capacitor electrode for suppression of leakage current inherently inhibits the oxygen diffusion into the lower electrode.

Regarding to claim 2, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 1 above, and Kim et al. further discloses wherein the atomic layer depositing occurs at a temperature of about 300 oC and at a pressure of about from 1-5 torr which fall into the ranged disclosed in claim 2 (Col. 10).

Regarding to claim 3, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 1 above, and Kim et al. further discloses wherein the

atomic layer has a thickness of about 60-70 A which falls into the ranged recited in claim 3 (line 39, Col. 5; lines 58, Col. 7).

Regarding to claim 4, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 1 above, and Kim et al. further discloses wherein the atomic layer contacts the first electrode.

Regarding to claim 5, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 1 above, and Kim et al. further discloses wherein the atomic layer comprises WN, TaN, TiN, RuOx, IrOx (lines 26-39, Col. 8).

Regarding to claim 6, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 1 above, and Fukuzumi et al. further discloses wherein the capacitor dielectric layer 52 is high dielectric constant material, for example, BaTiO3, SrTiO3, Ta2O5 (lines 1-25, Col. 17). It is well known in the art that these materials exhibit a K factor of greater than about 7 at 20 oC.

Regarding to claims 7, 38, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claims 1 and 34 above, and further disclose that at least one of the first or second electrodes comprise polysilicon (Fukuzumi et al.: Cols. 1-20; Kim et al.: Col. 1-10) and Fukuzumi et al. also discloses the dielectric layer comprises oxygen (Fukuzumi et al.: lines 1-25, Col. 17).

Regarding to claims 8, 39, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claims 1, 34 above, and Fukuzumi et al. further discloses wherein the capacitor dielectric layer 52 is high dielectric constant material, for example, (Ba,Sr)TiO3, BaTiO3, SrTiO3, Ta2O5 (lines 1-25, Col. 17).

Regarding to claim 11, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 1 above, and Fukuzumi et al. further discloses wherein the formation of the electrodes and the dielectric layer occur by other than atomic layer deposition (Fukuzumi et al.: Cols. 7-8).

Regarding to claim 12, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 1 above but fail to disclose the step of cleaning the first electrode prior to the atomic layer depositing by a method comprising HF dip, HF vapor clean, or NF3 remote plasma. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to clean the first electrode before perform ALD because the cleaning process would reduce contaminations, native oxide formed on the electrode surface in order to avoid unwanted reactions between contaminations and atomic depositing layers.

Regarding to claims 48, 62, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claims 1, 34 above and both further disclose wherein the substrate comprises a semiconductor wafer.

Regarding to claims 49-54, 63-68, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claims 1, 34 above and Kim et al. discloses wherein the first capacitor electrode comprises HSG polysilicon (Fukuzumi: lines 60-61, Col. 14; Kim:lines 23-27, Col. 1), the atomic layer comprises TiN (line 37, Col. 8) and both fail to disclose wherein the second electrode comprises the TiN. It would have been well known in the art that TiN is often used as capacitor electrode material. Fukuzumi et al. further discloses wherein the dielectric layer is a high K dielectric material. It would have been obvious to one having ordinary skill in the art that Al2O3 is suitable as a high K dielectric material since Al2O3 would have similar dielectric constant as those disclosed in Fukuzumi et al. and Kim et al.

Regarding to claim 35, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 34 and Kim et al. further discloses wherein the atomic layer conductive barrier layer is formed on the first electrode.

Regarding to claim 36, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 34 and Kim et al. further discloses wherein the atomic

layer comprises elemental metal, a metal alloy, or a metal-containing compound (lines 25-40, Col. 8).

Regarding to claim 37, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 34 and Kim et al. further discloses wherein the atomic layer comprises WN, TaN, TiN, RuOx (lines 25-40, Col. 8).

Regarding to claims 13, 40, Fukuzumi et al. discloses a method of forming a capacitor (See Fig. 33 and Cols. 1-20) comprising:

. forming a first capacitor electrode 51 over a substrate 1;

. forming a conductive barrier layer 52 over the first electrode (to prevent oxygen diffusion);

. forming a capacitor dielectric 53 over the barrier layer;

. forming a second capacitor electrode 54 over the dielectric layer.

Fukuzumi et al. fails to disclose the step of forming the conductive barrier layer involving the steps of forming a layer of first precursor at least one monolayer thick over the first electrode using chemisorbing method, and forming a second precursor at least one monolayer thick on the first precursor layer using chemisorbing method, a chemisorption product of the frist and second precursor layers being comprised by a layer of a conductive barrier material.

However, Kim et al. discloses the method of forming capacitor including the step of forming conductive barrier layer over the first capacitor electrode including the steps of forming a layer of first precursor 22 at least one monolayer thick over the first electrode using chemisorbing method, and forming a second precursor at least one monolayer thick on the first precursor layer using chemisorbing method (lines 55-59, Col. 2), a chemisorption product of the first and second precursor layers being comprised by a layer of a conductive barrier material 32 (Fig. 3D).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Fukuzumi et al. in view of Kim et al. by chemisorbing a layer of first and second precursors over the over the first capacitor electrode and reacting the chemisorption layers and reactants to form a conductive barrier layer because when chemisorbing method is performed where a high-purity film is formed by a plurality of atomic layers so that various reactants necessary for deposition of the film are sequentially supplied to the substrate by a gas pulsing method, a film having perfect step coverage is achieved, the thickness of the film can be easily adjusted (lines 5-30, Col. 4), the leakage current at lower electrode is suppressed, electric potential of device acts strongly while capable of obtaining cell capacitance enough for device operation and lower a soft error rate (lines 35-40, Col. 2). The conductive barrier layer formed over the first capacitor electrode for suppression of leakage current inherently inhibits the oxygen diffusion into the lower electrode.

Regarding to claims 14, 15, 16, 41, Fukuzumi et al. and Kim et al. discloses the claimed limitations as applied in claims 13, 40 above and Kim et al. further discloses wherein the first and second precursor layers each consist essentially of a monolayer, one or more chemical species and it is obvious that the precursor layers are saturated monolayers (layers 22, 24; lines 25-40, Col. 8).

Regarding to claim 17, Fukuzumi et al. and Kim et al. discloses the claimed limitations as applied in claim 13 above and Kim et al. further discloses wherein the first precursor is different from the second precursor (Cols. 6-7).

Regarding to claims 18, 19, 22, 42, 43, 45, Fukuzumi et al. and Kim et al. discloses the claimed limitations as applied in claims 13, 40 above and Kim et al. further discloses wherein the barrier layer comprises WN, TaN, TiN, RuOx (lines 25-40, Col. 8) (claims 22, 45). It is obvious to one having ordinary skill in the art that the first or second precursors comprises pairs such as WF6/NH3 because the reaction between the chemical in this pair would yield the same products that disclosed in Kim et al.

Regarding to claim 23, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 13 above, and Fukuzumi et al. further discloses wherein the capacitor dielectric layer 52 is high dielectric constant material, for example, BaTiO3, SrTiO3, Ta2O5 (lines 1-25, Col. 17). It is well known in the art that these materials exhibit a K factor of greater than about 7 at 20 oC.

Regarding to claims 24, 46, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claims 13 and 40 above, and further disclose that at least one of the first or second electrodes comprise polysilicon (Fukuzumi et al.: Cols. 1-20; Kim et al.: Col. 1-10) and Fukuzumi et al. also discloses the dielectric layer comprises oxygen (Fukuzumi et al.: lines 1-25, Col. 17).

Regarding to claims 25, 47, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claims 13, 40 above, and Fukuzumi et al. further discloses wherein the capacitor dielectric layer 52 is high dielectric constant material, for example, (Ba,Sr)TiO3, BaTiO3, SrTiO3, Ta2O5 (lines 1-25, Col. 17).

Regarding to claim 44, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 40 above, and Kim et al. further discloses wherein the conductive layer comprises elemental metal, a metal alloy, or a metal containing compound (Col. 8).

Regarding to claims 55, 69, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claims 13, 40 above and both further disclose wherein the substrate comprises a semiconductor wafer.

Regarding to claims 56-61, 70-75, Fukuzumi et al. and Kim et al. disclose the claimed limitations as applied in claim 40 above and Kim et al. discloses wherein the

first capacitor electrode comprises HSG polysilicon (Fukuzumi: lines 60-61, Col. 14; Kim:lines 23-27, Col. 1), the atomic layer comprises TiN (line 37, Col. 8) and both fail to disclose wherein the second electrode comprises the TiN. It would have been well known in the art that TiN is often used as capacitor electrode material. Fukuzumi et al. further discloses wherein the dielectric layer is a high K dielectric material. It would have been obvious to one having ordinary skill in the art that Al2O3 is suitable as a high K dielectric material since Al2O3 would have similar dielectric constant as those disclosed in Fukuzumi et al. and Kim et al.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

Conclusion

For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

Claims 1-8, 10-25, and 3-75 are still rejected, and the previous rejection is presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See

MPEP ' 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le
Examiner
Art Unit 2818